Correct-by-Construct Netlist Based Integration Flow for Mixed-Signal Low Power Multi Chip Module

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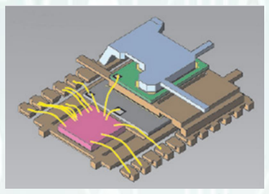
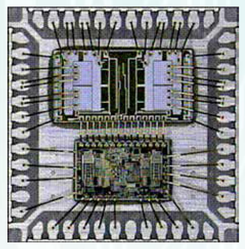
1. Introduction

- Several emerging markets require complex functionality with platform flexibility in an SoC
- Many analog power delivery, analog signal path and RF signal chain functions can benefit from existing ICs in older technology
- MCM[1] can provide a means for quicker time to market
  - Focus on development of differentiating new functions, accrue benefits from newer technology nodes through higher integration density, performance and lower power



Stacked FET with drivers[1]



2D package, 2 dies connected to package & interconnected with bond wires[1]

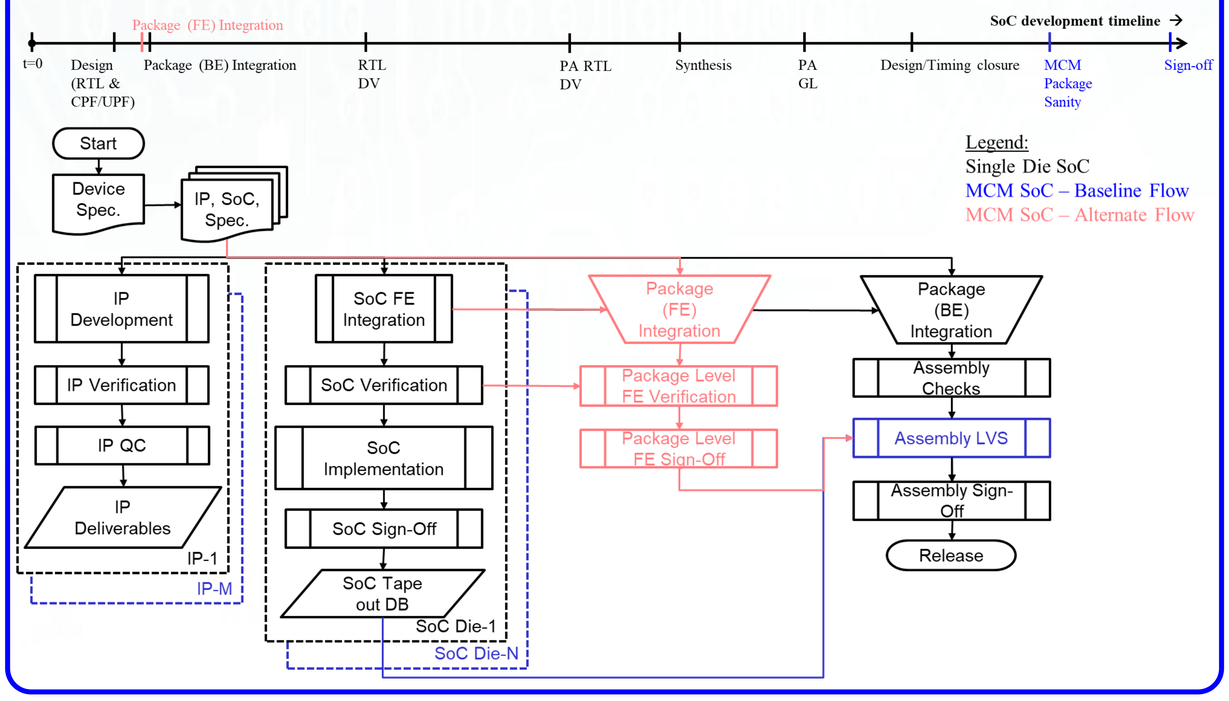
3D package, dies stacked on top of each other & interconnected with bond wires[1]

Source: [1] Sreenivasan Koduri, "3D packaging for analog and power products", Chip Scale Review, May-June 2014

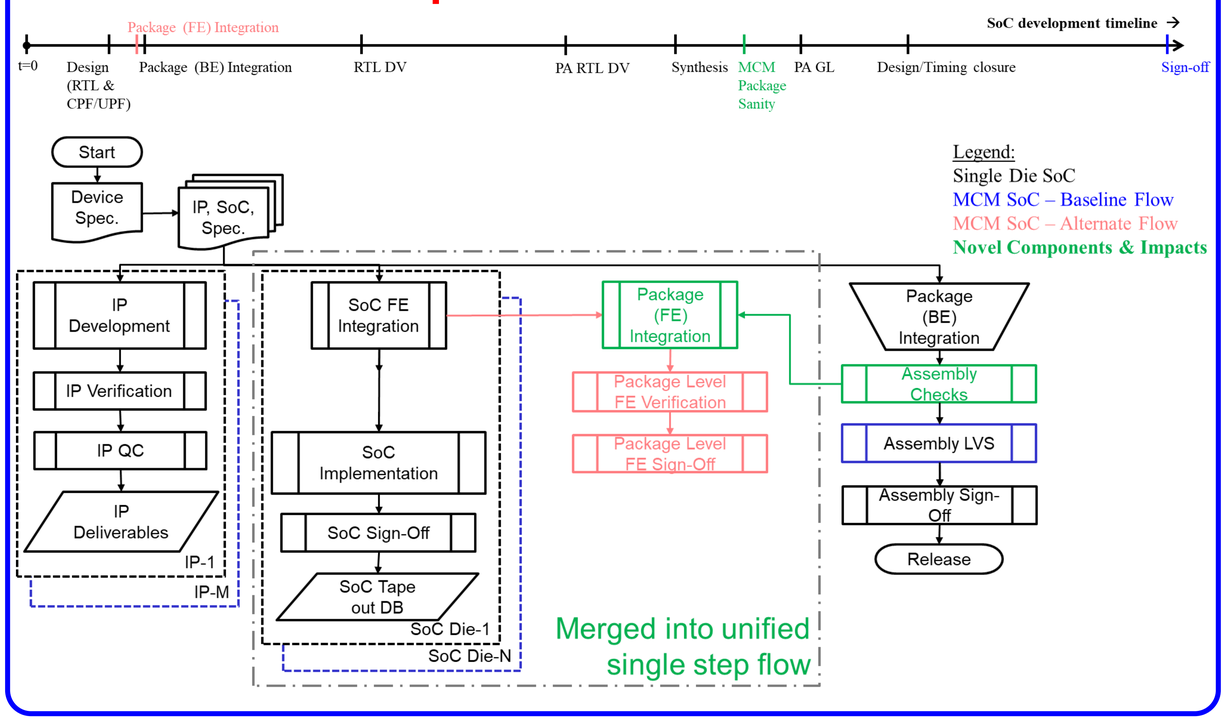
2. Motivation & Problem Statement

- Current MCM technologies involve independent development, verification and validation of different chips
  - Results in manual MCM integration
  - Lack of environment and capability for integrated MCM level verification for complex low power mixed-signal SoCs
  - Late findings of MCM level integration issues at LVS stage can throw surprises
  - Analog on Top integration methods mitigate some concerns due to a unified schematic frontend
    - Need MCM level LVS for equivalence between schematic and final IC layout and MCM package physical design
- This work presents a novel solution for an automated MCM netlist generation from package level integration information
  - Avoids a need for MCM level LVS at mature design stages
  - Extends correct-by-construct approach

3. Conventional MCM IC Design Flow



4. Main Idea: Proposed Solution Framework



5. Enabling Features

- Enabled by extension to existing assembly rule check tool
- Generate different MCM netlist abstractions needed for early frontend verification including low power AMS co-sim. and LVS
  - Verilog netlist for MCM level → Starting point for SoC verification (DMS and AMS co-sim).
  - Power intent (CPF or UPF) for MCM level
  - Package/bond wire related fault list[2] → Mixed-signal fault simulation
    - Conventional fault simulation flows results in $O(N^2)$ short faults for N wire bonded interfaces
    - This flow generates an optimal & realistic fault list of size O(N) (k*N, k<<N-1)
- Avoid Independent SoC level DV setup and flow
  - Each SoC is verified in MCM context
- Avoid MCM level LVS

Source: [2] Lakshmanan Balasubramanian, et al, "Applications of Analog Defect Simulation to Digital, Memory, ADC and Package Level Tests," 31st Microelectronics Design and Test Symposium (MDTS), May, 2022

6. Industrial Interception

- Applied in embedded processing, low power, mixed-signal SoC
  - Legacy die, a power managed mixed-signal SoC → Treated like any other conventional hard IP[3,4]
    - All associated design artefacts including functional, timing, power intent and circuit level abstractions
  - New SoC for 2nd die for low power mixed-signal MCU and digital sub-system
    - Both at RTL and post implementation gate level (GL) stages
- Auto generation of integration netlists from package level integration
  - Usually available at early design stage
- Avoided SoC level DV environment
- Only MCM level DV environment (DMS and AMS co-sim.)
- First ever time MCM level verification enabled, and early in design cycle with no additional manual effort for verification setup
  - Avoided dependency on late LVS

Source: [3] Aswani Kumar Golla, et al, "Hierarchical Power Intent Driven Efficient Power Integration Methodology for Ultra Low Power Mixed-Signal SoC,", DAC 2019
[4] Vijay Kumar Sankaran, et al, "Modern Recipes for Brewing the Inevitable Methodology for Today's ICs: Low-Power Mixed-Signal Design Verification", DAC 2019

7. Evidence and Results

- **Critical design issues found** by pre-silicon verification and fixed
- Missing isolation required on die 2 for a signal crossing between different power domains across dies
- An analog design issue
  - On-chip low dropout voltage regulator (LDO) in legacy die supplying a portion of new die
  - Output settling issue at low power mode identified in MCM level AMS co-sim.
- Device successfully released for customer sample after silicon validation, with first pass silicon success

8. Conclusions

- There has been an increasing need for MCM integration to provide low cost solutions, at faster time-to-market
- Several businesses within TI in the recent past resorted to MCM based products
- Conventional MCM integration flow involves manual integration for FE and BE
- Integration consistency validated at a pretty late design stage through an LVS
- For embedded processing design using digital-on-top (DoT) flows, even LVS based validation is not done → Only manual reviews
  - Potential for avoidable quality issues, affecting our ability to monetize the efforts and related costs
- An automation method implemented → Enables **correct-by-construct MCM integration & verification**, avoids dependency on late maturing LVS flow for identifying MCM level integration issues
- Successfully, tactically intercepted in an embedded processing, low power, mixed-signal SoC integrated with a legacy physical layer die in an MCM
- Future scope
  - Strategic, broad use for all future MCM devices planned
  - Extension for UPF Power Model generation

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